REVIEW PAPER ON REVERSIBLE LOGIC GATE

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Abstract:

In the recent years reversible logic has played important role in research areas for power optimization with its application in Low power CMOS, optical information processing, quantum computing and nano technology. Reversibility plays a fundamental role when computations with minimal energy dissipations are considered. The fundamental logic gates, such as NAND, AND, NOR, XOR and XNOR gates are not reversible. In this paper, literature survey based on various research papers of reversible logic circuits is presented and future scope regarding reversible logic is discussed. The main purpose of designing the reversible logic is to decrease the quantum cost, depth of the circuits and the number of garbage outputs. Future digital technology will use reversible logic gates in order to reduce the power consumption and propagation delay as it effectively provides negligible loss of information in the circuit.

Keywords:

Reversible logic gates, quantum cost, garbage output and power dissipation**.**

1. INTRODUCTION

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. The loss of information is associated with laws of physics describing that one bit of information lost dissipates kTln2 of energy, where k is Boltzmann' constant and T is the temperature of the system [2]. Reversibility in computing implies that information about the computational states should never be lost. The reversible logic is either physical reversible or logical reversible. Reversibility in computing implies that no information about the computational states can never be lost, so we can recover any earlier stage by computing backward or un-computing the results. This is known as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no heat in terms of wastage of energy [1]. Various parameters of reversible logic gates are used to design the work.

Reversible logic gate is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. A reversible gate is also defined as a bijective Boolean function from n to n values. Let the input vector be Iv, output vector Ov and they are defined as follows,

Iv = (Ii, Ii+1, Ii+2 …In-1, In) and Ov = (Oi, Oi+1, Oi+2 … On-1, On). For each particular i, there exits the relationship **Iv = Ov** [10]

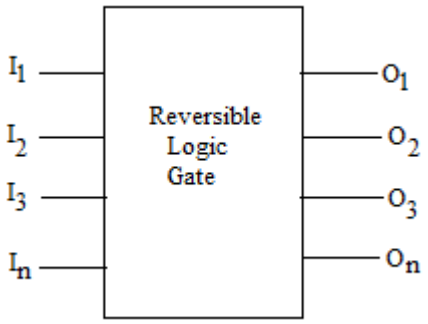

Fig. 1. Symbol of Reversible logic gate with n*n input and output

In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit.

- Garbage outputs must be minimum.
- Minimum delay.
- Loops or feedbacks are not permitted.
- Minimum quantum cost.
- Fan-out is not permitted.

2. LITERATURE SURVEY

In 1961, R.Landauer described that the logical irreversibility is associated with physical irreversibility and requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In conventional system the millions of gates used to perform logical operations. Author proved that heat dissipation avoidable if system made reversible [1].

In 1973, C.H.Bennett described that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Reversible gate can generate unique output vector from each input vector and vice versa [2].

In 2011, Md.Mazder Rahman et.al presented a quantum gate library that consists of all possible two-Qubit quantum gates which do not produce entangled states. These gates are used to reduce the quantum cost of reversible circuits. They proposed a two-qubit quantum gate library that plays a significant role in reducing the quantum cost of reversible gates [3].

In 2012, B.Raghu kanth et Al described the comparison between the reversible and conventional logic gates. The author compared the 4-bit reversible adder/subtractor circuit using DKG gate. The comparison is carried out in terms of low power consumption, lesser delay, number of gates, garbage outputs and constant inputs. The results of this adder/subtractor circuit using DKG gate was better as compared to existing one and this adder/subtractor circuit can be applied to the design of complex systems in nanotechnology. The author explained that a 4*4 reversible DKG gate can work singly as a reversible full adder and a reversible full subtraction [4]

In 2013, Partik Kumar Bhatt described the reversible comparator which is implemented with the Reversible BVN gate. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. The implementing of this comparator has advantages of reducing the number of garbage outputs, gate count and number of constant input and quantum cost. [5]

In 2014, A.Anjana, designed the RS Flip-Flop using Reversible logic gate which is implemented by cascading the Toffoli gate and TNORG gate. The paper emphasis on the comparison of gates in term of power and delay .By using reversible logic gates power consumption was estimated 52mW & path delay was about 6.991ns which was very less as compare to using

conventional gate. The number of gates is reduced from 6 to 2 as compared to the existing module. [6]

In 2014, Ashima Malhotra, et.al, proposed different types of reversible multiplexers using modified Fredkin gate. They were proposed 2:1, 4:1, 8:1 and 16:1 reversible multiplexers. They were also compared with quantum cost and power consumption of proposed reversible multiplexers with existing one. [7]

In 2014, Manjeet Singh Sankhwar et.al described the design of High speed low power reversible logic BCD adder which is implemented using HNG gate. This BCD adder is specially designed to make it suitable for the reversible logic implementations. This design strategy reduces the most important factor of the reversible circuit cost and the number of gates. Also in this research, a known traditional logic implementation for BCD adder was modified to get a delay reduction for multi-digit addition. [8]

In 2014, Ashima Malhotra et.al described that reversible modified Fredkin gate used to design the multiplexers with low quantum cost and compare it with existing work. They also compare the quantum cost of multiplexers design using Fredkin gate with Modified Fredkin gate used to design he multiplexers [9].

In 2015, Sukhjeet kaur, et.al, proposed different types of reversible encoders using Feynman and Fredkin gate. They were proposed 4:2, 8:3 and 16:4 reversible encoders. They were also compared with quantum cost of proposed reversible multiplexers with existing one. [10]

In 2015, Manjinder Pal Singh,et al, proposed different types of reversible decoders using BVF, F2G and FRG gates. They were proposed 2:4, 3:8 and 4:16 reversible decoders. They were also compared with quantum cost and hardware complexity of proposed reversible multiplexers with existing one. The reversible logic circuits can also be designed with less area and delay. [11]

3. DESIGN OF REVERSIBLE LOGIC GATES

The various types of reversible logic gates used commonly are explained below:

3.1 Feynman Gate

Fig 2.1a shows the Feynman gate which is a 2*2 gate and is also called as Controlled NOT gate and it is widely used as a copying gate because fan-out is not allowed in reversible logic. The inputs (A, B) and outputs P=A, Q= A XOR B. It has Quantum cost one.

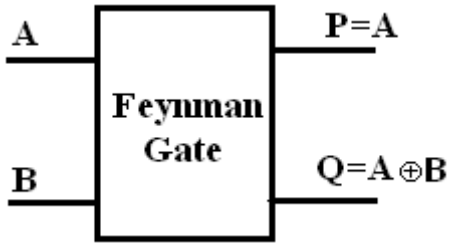

Fig..2(a). Feynman Gate – 2*2 gate

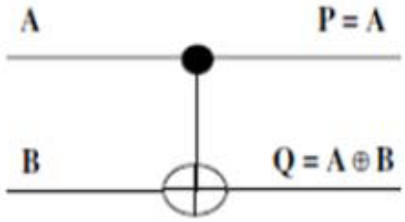

Fig. 2(b). Quantum implementation of Feynman Gate

3.2 Toffoli Gate

Fig 3.1a shows a Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A,Q=B, R=AB XOR C. It has Quantum cost five.

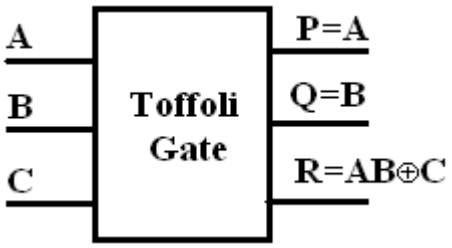

Fig. 3(a). Toffoli Gate – 3*3 gate

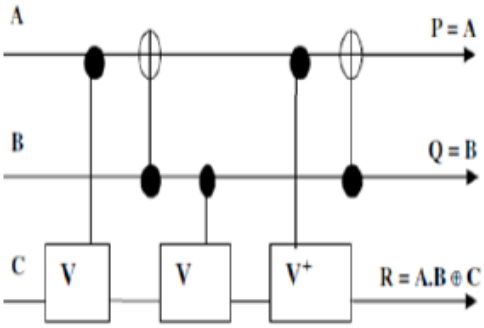

Fig. 3(b). Quantum implementation of Toffoli Gate

3.3 Fredkin Gate

Fredkin gate is 3x3 gate with input vector is I(A,B,C) and the output vector is O(P,Q,R).The output is P=A,Q=A'B+AC and R=A'C+AB. Quantum cost of Fredkin gate is 5.

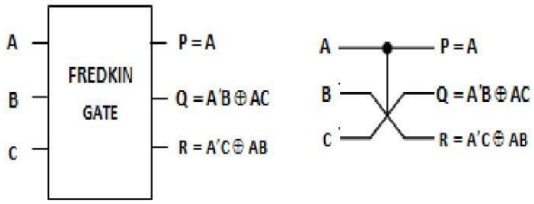

Fig. 4. Fredkin Gate – 3*3 gate & its quantum implementation

3.4 Peres Gate

Fig 5.1a shows a Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs P = A ,Q = A XOR B, R = AB XOR C. Since it requires 1 V+, 2 V & 1 CNOT gate, it has the Quantum cost of four.

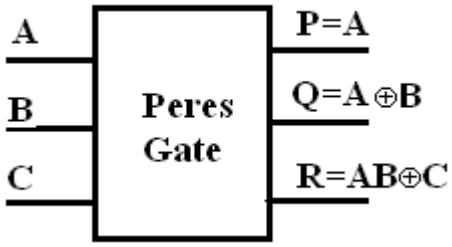

Fig. 5(a). Peres Gate – 3*3 gate

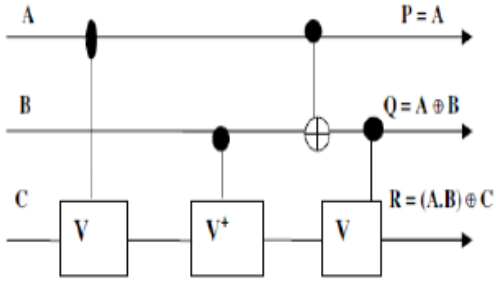

Fig. 5(b). Quantum implementation of Peres Gate

3.5 New BJN Gate

Its a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R =(A+B) XOR C. Its quantum realization is shown in figure 6.2b. It has quantum cost of 5.

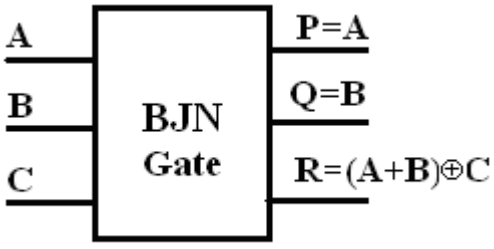

Fig. 6(a). BJN Gate - 3*3 gate

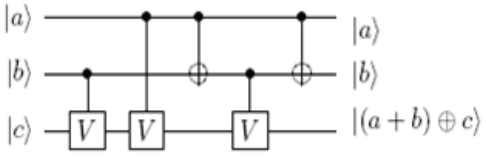

Fig. 6(b). Quantum realization of BJN gate

3.6 TR Gate

The fig 7.1 a shows a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=A XOR B, R= AB' XOR C. It has Quantum cost six.

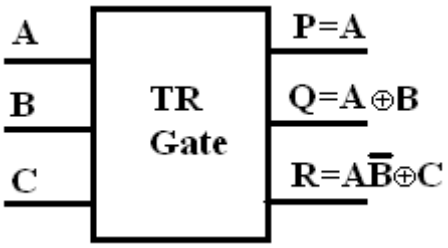

Fig. 7(a). TR Gate - 3*3 gate

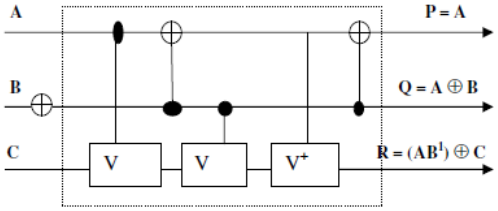

Fig. 7(b). Quantum implementation of TR Gate

4. PARAMETERS RELATETED TO REVESIBLE GATES

4.1 Gate count: The number of reversible gates used to realize the function.

4.2 Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.

4.3 Quantum cost: This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Quantum gates have some property given in equation 1, 2 and 3.

1. V*V=NOT
2. V*V+ =V+*V=1
3. V+*V+=NOT

4.4 Gate levels: This refers to the number of levels in the circuit which are required to realize the given logic functions.

4.5 Garbage Output: Unwanted output of reversible gate is called garbage output. The output of reversible gate is not used as a primary output or as input to other gates is called garbage output. Garbage's outputs are needed in circuit to maintain reversibility concept. Figure 8 shows an example of reversible function of f = x1x2 XOR x3, the two unused pins are the garbage outputs.

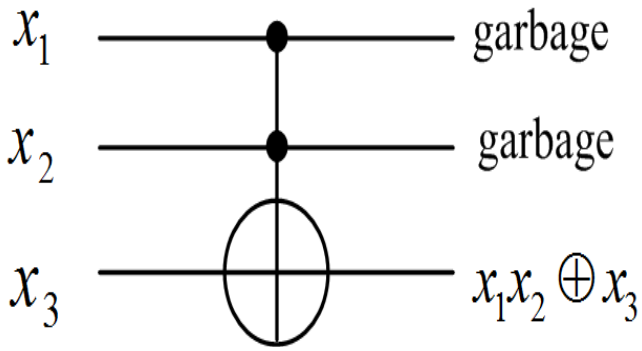

Fig. 8. Garbage Output

4.6 Hardware Complexity: Hardware Complexity refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit.

5. CONCLUSIONS AND FUTURE WORK

Reversible circuit is an emerging technology with a promising application because of low power dissipation. The centers of this paper are the different kinds of reversible gates and its various parameters. In future, by using these gates we can design any of combinational or sequential circuit with numerous advantages over conventional gates such as, low power, low complexity, less delay, high speed etc. Reversible computing is becoming an important research area include Quantum computing, Nanotechnology, Low power CMOS design, Spacecraft, Cryptography, Digital signal processing.

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